In the Specification

At page 1, please replace the TITLE as follows (underlined denotes replacements additions and strikethough notes deletions):

METHOD AND APPARATUS FOR ENCODING FRAMES OF IMAGE DATA AT A VARYING QUALITY LEVEL

At page 6, lines 3 – 11, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

FIG. 2 illustrates another embodiment of an encoding arrangement 300 that is particularly suited for use in the present invention. An original image is stored in a memory 301, such as a frame buffer. The original image is received by a summing element 302, which is configured and arranged to calculate ~~difference~~different information representing the difference between the original image and an image stored in a memory 304, such as a frame buffer. When no image is initially stored in the memory 304, the original image is passed to a transformation block 306, which transforms the image into coefficient data selected from a continuous range of values. In the illustrated example, the transformation block 306 performs a discrete cosine transform (DCT) on the original image.

At page 8, lines 26 – 30 and page 9, lines 1 – 8 , please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

The encoding arrangement 300 of FIG. 2 can be implemented using any of a variety of processor arrangements, including the arrangements disclosed in connection with U.S. patent application numbers 08/692,993, now U.S. patent number 5,901,248 and 08/658,917, respectively entitled and relating to issued patents also entitled "Programmable Architecture and Methods for Motion Estimation" (patent number 5,594,813) and "Video Compression and Decompression Processing and Processors" (patent number 5,379,351), and also in connection with application number 09/095,448 entitled "Videocommunicating Device with an On-screen Telephone Keypad User-Interface Method and Arrangement." These applications and issued

patents are incorporated herein by reference. Such processor arrangements are based on a multi-processor chip having uniquely arranged RISC and DSP type processors, which can be selectively loaded with program code for decoding and encoding video data of various formats. In yet another embodiment, the encoding arrangement may be implemented with ASICs.

At page 10, lines 14 – 19, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

FIGS. 4A-4B illustrate an example embodiment of a method for encoding frames of video data using selected ranges of quantization levels. At step [[402]]502 a first frame is received for encoding, and an initial range of quantization levels is selected at step 504. The selected quantization range may be selected to accommodate a desired resolution and available bandwidth for the initial frame, considering that all blocks are encoded and transmitted for the initial frame.

At page , lines 14 – 19, please replace the paragraph as follows (underlined denotes replacements additions and strikethough notes deletions):

If the quantization range for skipped blocks is selected, control is directed to step to initialize the block counter to reference the first block in the list of skipped blocks and to step 550 to get block i from the list of skipped blocks. At step 552, the block is encoded and transmitted using a quantization level selected from the quantization range for skipped blocks. The particular quantization level can be selected using conventional methods. Step [[556]]554 decodes and stores the decoded block, and the block counter is incremented at step 556. Once all the skipped blocks have been processed, decision step 558 returns control to step 526 to get the next frame.